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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Group Art Unit: Unassigned
Examiner: Unassigned

In Re PATENT APPLICATION Of:

Applicant(s) : Shigayuki UEDA)
Serial No. : Divisional of Appl. Serial No. 09/665,663)
Filed : March 22, 2004) **INFORMATION**
For : SEMICONDUCTOR CHIP AND METHOD OF) **DISCLOSURE**
PRODUCING THE SAME)
Attorney Ref. : AI 281 D1) _____

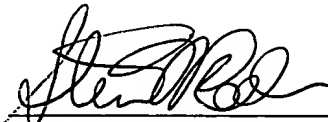
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the duty of disclosure, attached is a copy of the Form PTO-1449 from the parent application, serial number, **09/665,663**, which the Examiner may wish to consult during examination of this Divisional Application thereof.

Respectfully submitted,

April 14, 2004
Date


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SMR:tl

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FORM PTO-1449 INFORMATION DISCLOSURE STATEMENT				Atty. Docket		Application No.	
				AI 281		09/665,663	
				Applicant Shigeyuki UEDA			
				Filing Date September 20, 2000		Group 2823	
U.S. PATENT DOCUMENTS							
Examiner Initial		Document Number	Date	Name	Class	Sub-Class	Filing Date
	AA						
	AB						
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
FOREIGN PATENT DOCUMENTS							
		Document Number	Date	Country	Class	Sub-Class	Translation
	AI	11-121509	4/30/99	JAPAN			Yes
	AJ	11-135714	5/21/99	JAPAN			Yes
	AK						
	AL						
	AM						
	AN						
OTHER (Including Author, Title, Date, Pertinent Pages, etc.)							
	AO						
Examiner					Date Considered		
EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.							